We Claim:

1. A method for testing a plurality of integrated circuits, including the steps of:

performing a plurality of tests on the plurality of integrated circuits;

identifying integrated circuits that failed at least one of the plurality of tests and identifying tests failed by the integrated circuits; and

repeating at least one identified failed test on the identified integrated circuits.

2. A method for testing according to claim 1, wherein each of the plurality of integrated circuits has a corresponding unique integrated circuit identifier stored in a memory and each of the plurality of tests has an associated test identifier, and wherein the step of identifying further includes the step of:

storing failed test identifiers in the memory in association with the failed integrated circuit identifiers.

3. A method for testing according to claim 2, wherein the step of repeating includes selecting tests to be repeated by retrieving at least one of the stored failed test identifiers.

4. A method for testing according to claim 3, wherein each failed integrated circuit has a set of associated failed test identifiers stored in the memory, and wherein the step of selecting includes:

comparing sets of failed test identifiers for each of the failed integrated circuits;

selecting a subset of tests that includes at least one test from each set of failed test identifiers; and

repeating the subset of tests on the failed integrated circuits.

5. A method for testing according to claim 4, wherein the step of selecting a subset of tests includes the steps of:

determining an amount of time each test requires;

summing the determined amounts of time for a plurality of combinations of tests; and

selecting the combination of tests that requires a minimal amount of time.

6. A method for testing according to claim 4, wherein the step of selecting a subset of tests includes the steps of

ranking the identified failed tests in order of the highest number of integrated circuits failing each test; and

selecting the highest ranked test to be in the subset of tests.

7. A method for testing according to claim 6, further including the steps of:

ranking the identified failed tests for each of the remaining failed integrated circuits that did not fail the first of said ranked tests in order of the highest number of integrated circuits failing each of said remaining failed tests;

selecting the highest ranked test, of said identified failed tests for each of the remaining integrated circuits, to be in the subset of tests; and

repeating the steps of ranking and selecting until there are no identified circuits that did not fail at least one of the tests in the subset of tests.

8. A method for testing according to claim 1 wherein the integrated circuits each include an array of memory cells and wherein the step of repeating includes the substep of identifying at least one failed memory cell in the array of memory cells for each identified integrated circuit.

9. A method for testing as recited in claim 8, further including the step of repairing the identified at least one failed memory cell in each identified integrated circuit.

10. A method for testing an integrated circuit having an array of memory cells and an associated integrated circuit identifier stored in a memory, the method including the steps of:

performing a first test on the integrated circuit, the first test having an associated first test identifier;

determining whether the integrated circuit passed the first test;

storing a first test identifier in the memory in association with the integrated circuit identifier when the integrated circuit did not pass the first test;

reading test identifiers stored in the memory that are associated with the integrated circuit identifier; and

repeating at least one test associated with the read test identifiers for the first memory chip.

11. The method for testing according to claim 10, further including the steps of:

performing a second test on the integrated circuit when the integrated circuit passes the first test;

determining whether the integrated circuit passed the second test; and

storing a second test identifier in the memory in association with the integrated circuit identifier when the integrated circuit did not pass the second test.

12. The method for testing according to claim 10, wherein the step of performing a first test includes performing a plurality of tests each having an associated test identifier and

wherein the step of determining includes determining whether the integrated circuit failed any one of the plurality of tests, wherein the step of storing includes storing a corresponding test identifier in association with an integrated circuit identifier for each failed test, and wherein the test of repeating includes repeating at least one of the tests failed by each failed integrated circuit.

13. The method for testing according to claim 12, wherein each failed integrated circuit has a set of associated failed test identifiers stored in the memory, and wherein the step of selecting includes:

comparing sets of failed test identifiers for each of the failed integrated circuits;

selecting a subset of tests that includes at least one test from each set of failed test identifiers; and

repeating the subset of tests on the failed integrated circuits.

14. A method for testing according to claim 13, wherein the step of selecting a subset of tests includes the steps of:

determining an amount of time each test requires;

summing the determined amounts of time for a plurality of combinations of tests; and

selecting the combination of tests that requires a minimal amount of time.

15. A method for testing according to claim 13, wherein the step of selecting a subset of tests includes the steps of

ranking the identified failed tests in order of the highest number of integrated circuits failing each test; and

selecting the highest ranked test of said identified failed tests for each of the remaining integrated circuits to be in the subset of tests.

16. A method for testing according to claim 15, further including the steps of:

ranking the identified failed tests for each of the remaining failed integrated circuits that did not fail the first of said ranked tests in order of the highest number of integrated circuits failing each of said remaining failed tests;

selecting the highest ranked test, of said identified failed tests for each of the remaining integrated circuits, to be in the subset of tests; and

repeating the steps of ranking and selecting until there are no identified circuits that did not fail at least one of the tests in the subset of tests.

17. An apparatus for testing a plurality of integrated circuits, including:

means for performing a plurality of tests on the plurality of integrated circuits;

means for identifying integrated circuits that failed at least one of the plurality of tests and identifying tests failed by the integrated circuits; and

means for repeating at least one identified failed test on the identified integrated circuits.

18. An apparatus for testing according to claim 17, wherein each of the plurality of integrated circuits has a corresponding unique integrated circuit identifier stored in a memory and each

of the plurality of tests has an associated test identifier, and wherein the means for identifying further includes:

means for storing failed test identifiers in the memory in association with the failed integrated circuit identifiers.

19. An apparatus for testing according to claim 18, wherein the means for repeating includes means for selecting tests to be repeated by retrieving at least one of the stored failed test identifiers.

20. An apparatus for testing according to claim 19, wherein each failed integrated circuit has a set of associated failed test identifiers stored in the memory, and wherein the means for selecting includes:

means for comparing sets of failed test identifiers for each of the failed integrated circuits;

means for selecting a subset of tests that includes at least one test from each set of failed test identifiers; and

means for repeating the subset of tests on the failed integrated circuits.

21. An apparatus for testing according to claim 20, wherein the means for selecting a subset of tests includes:

means for determining an amount of time each test requires;

means for summing the determined amounts of time for a plurality of combinations of tests; and

means for selecting the combination of tests that requires a minimal amount of time.

22. An apparatus for testing according to claim 20, wherein the means for selecting a subset of tests includes:

means for ranking the identified failed tests in order of the highest number of integrated circuits failing each test; and

means for selecting the highest ranked test to be in the subset of tests.

23. An apparatus for testing according to claim 22, further including:

means for ranking the identified failed tests for each of the remaining failed integrated circuits that did not fail the first of said ranked tests in order of the highest number of integrated circuits failing each of said remaining failed tests;

means for selecting the highest ranked test, of said identified failed tests for each of the remaining integrated circuits, to be in the subset of tests; and

means for repeatedly activating the means for ranking and selecting until there are no identified circuits that did not fail at least one of the tests in the subset of tests.

24. An apparatus for testing according to claim 17 wherein the integrated circuits each include an array of memory cells and wherein the means for repeating includes a means for identifying at least one failed memory cell in the array of memory cells for each identified integrated circuit.

25. An apparatus for testing as recited in claim 24, further including a means for repairing the identified at least one failed memory cell in each identified integrated circuit.

26. An apparatus for testing an integrated circuit having an array of memory cells and an associated integrated circuit identifier stored in a memory, including:

means for performing a first test on the integrated circuit, the first test having an associated first test identifier;

means for determining whether the integrated circuit passed the first test;

means for storing a first test identifier in the memory in association with the integrated circuit identifier when the integrated circuit did not pass the first test;

means for reading test identifiers stored in the memory that are associated with the integrated circuit identifier; and

means for repeating at least one test associated with the read test identifiers for the first memory chip.

27. An apparatus for testing according to claim 26, further including:

means for performing a second test on the integrated circuit when the integrated circuit passes the first test;

means for determining whether the integrated circuit passed the second test; and

means for storing a second test identifier in the memory in association with the integrated circuit identifier when the integrated circuit did not pass the second test.

28. An apparatus for testing according to claim 26, wherein the means for performing a first test includes means for performing a plurality of tests each having an associated test identifier and wherein the means for determining includes means for determining whether the integrated circuit failed any one of the plurality of tests, wherein the means for storing includes means for storing a corresponding test identifier in association with an integrated circuit identifier for each failed test, and wherein the test of repeating includes means for repeating at least one of the tests failed by each failed integrated circuit.

29. An apparatus for testing according to claim 18, wherein each failed integrated circuit has a set of associated failed test identifiers stored in the memory, and wherein the means for selecting includes:

means for comparing sets of failed test identifiers for each of the failed integrated circuits;

means for selecting a subset of tests that includes at least one test from each set of failed test identifiers; and

means for repeating the subset of tests on the failed integrated circuits.

30. An apparatus for testing according to claim 29, wherein the means for selecting a subset of tests includes:

means for determining an amount of time each test requires;

means for summing the determined amounts of time for a plurality of combinations of tests; and

means for selecting the combination of tests that requires a minimal amount of time.

31. An apparatus for testing according to claim 29, wherein the means for selecting a subset of tests includes:

means for ranking the identified failed tests in order of the highest number of integrated circuits failing each test; and

means for selecting the highest ranked test to be in the subset of tests.

32. An apparatus for testing according to claim 31, further including:

means for ranking the identified failed tests for each of the remaining failed integrated circuits that did not fail the first of said ranked tests in order of the highest number of integrated circuits failing each of said remaining failed tests;

means for selecting the highest ranked test, of said identified failed tests for each of the remaining integrated circuits, to be in the subset of tests; and

means for repeatedly activating the means for ranking and selecting until there are no identified circuits that did not fail at least one of the tests in the subset of tests.